What is claimed is:

1. A semiconductor device, comprising:

an isolation region located in a substrate;

an NMOS device located partially over a surface of the substrate; and

a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface;

wherein a first one of the NMOS and PMOS devices includes one of:

first source/drain regions recessed within the surface; and

first source/drain regions extending from the surface; and

wherein a second one of the NMOS and PMOS devices includes one of:

second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface;

second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and

second source/drain regions substantially coplanar with the surface.

2. The semiconductor device of claim 1 wherein:

a high-gate one of the NMOS and PMOS devices includes a first gate interposing associated source/drain regions and having a first height over the surface; and

a low-gate one of the NMOS and PMOS devices includes a second gate interposing associated source/drain regions and having a second height over the surface, wherein the first height is substantially greater than the second height.

3. The semiconductor device of claim 1 wherein:

a wide-spacer one of the NMOS and PMOS devices includes a first gate interposing associated source/drain regions and first spacers on opposing sides of the first gate, the first spacers each extending from the first gate to a first width; and

a narrow-spacer one of the NMOS and PMOS devices includes a second gate interposing associated source/drain regions and second spacers on opposing sides of the second gate, the second spacers each extending from the second gate to a second width, wherein the first width is substantially greater than the second width.

4. The semiconductor device of claim 2 wherein:

a wide-spacer one of the NMOS and PMOS devices includes first spacers on opposing sides of an associated one of the first and second gates, the first spacers each extending from the associated gate to a first width; and

a narrow-spacer one of the NMOS and PMOS devices includes second spacers on opposing sides of an associated one of the first and second gates, the second spacers each extending from the associated gate to a second width, wherein the first width is substantially greater than the second width.

5. The semiconductor device of claim 1 wherein at least one set of the first and second source/drain regions comprises SiGe.

6. The semiconductor device of claim 1 wherein at least one set of the first and second source/drain regions comprises SiC.

7. The semiconductor device of claim 6 wherein at least one set of the first and second source/drain regions comprise SiGe.

8. The semiconductor device of claim 1 wherein the substrate has a <110> crystal orientation.

9. The semiconductor device of claim 1 wherein the substrate has a <100> crystal orientation.

10. The semiconductor device of claim 1 wherein the substrate is a silicon-on-insulator substrate.

11. The semiconductor device of claim 1 wherein the substrate is a bulk silicon substrate.

12. The semiconductor device of claim 1 wherein at least one set of the first and second source/drain regions comprises strained source/drain regions.

13. The semiconductor device of claim 2 wherein at least one set of the first and second source/drain regions comprises strained source/drain regions.

14. The semiconductor device of claim 3 wherein at least one set of the first and second source/drain regions comprises strained source/drain regions.

15. The semiconductor device of claim 1 further comprising an etch stop layer located over the NMOS and PMOS devices and imparting a first stress in the first source/drain regions and a second stress in the second source/drain regions, wherein the first and second stresses are substantially different in magnitude.

16. A semiconductor device, comprising:

an isolation region located in a substrate;

an NMOS device located partially over a surface of the substrate; and

a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface;

wherein a first one of the NMOS and PMOS devices includes:

first source/drain regions located at least partially in the substrate; and

a first gate interposing the first source/drain regions and having a first gate height over the surface; and

wherein a second one of the NMOS and PMOS devices includes:

second source/drain regions located at least partially in the substrate; and

a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different.

17. The semiconductor device of claim 16 wherein:

a wide-spacer one of the NMOS and PMOS devices includes first spacers on opposing sides of an associated gate, the first spacers each extending from the associated gate to a first width; and

a narrow-spacer one of the NMOS and PMOS devices includes second spacers on opposing sides of an associated gate, the second spacers each extending from the associated gate to a second width, wherein the first width is substantially greater than the second width.

18. The semiconductor device of claim 16 wherein at least one set of the first and second source/drain regions comprises SiGe.

19. The semiconductor device of claim 16 wherein at least one set of the first and second source/drain regions comprises SiC.

20. The semiconductor device of claim 19 wherein at least one set of the first and second source/drain regions comprises SiGe.

21. The semiconductor device of claim 16 wherein the substrate has a <110> crystal orientation.

22. The semiconductor device of claim 16 wherein the substrate has a <100> crystal orientation.

23. The semiconductor device of claim 16 wherein the substrate is a silicon-on-insulator substrate.

24. The semiconductor device of claim 16 wherein the substrate is a bulk silicon substrate. .

25. The semiconductor device of claim 16 wherein at least one set of the first and second strained source/drain regions comprises strained source/drain regions.

26. The semiconductor device of claim 17 wherein at least one set of the first and second strained source/drain regions comprises strained source/drain regions.

27. The semiconductor device of claim 16 further comprising an etch stop layer located over the NMOS and PMOS devices and imparting a first stress in the first source/drain regions and a second stress in the second source/drain regions, wherein the first and second stresses are substantially different in magnitude.

28. A semiconductor device, comprising:

an isolation region located in a substrate;

an NMOS device located partially over a surface of the substrate; and

a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface;

wherein a first one of the NMOS and PMOS devices includes:

first source/drain regions located at least partially in the substrate;

a first gate interposing the first source/drain regions; and

first spacers on opposing sides of the first gate and each extending from the first gate to a first width; and

wherein a second one of the NMOS and PMOS devices includes:

second source/drain regions located at least partially in the substrate;

a second gate interposing the second source/drain regions; and

second spacers on opposing sides of the second gate and each extending from the second gate to a second width, wherein the first and second widths are substantially different.

29. The semiconductor device of claim 28 wherein at least one set of the first and second source/drain regions comprises SiGe.

30. The semiconductor device of claim 28 wherein at least one set of the first and second source/drain regions comprises SiC.

31. The semiconductor device of claim 30 wherein at least one set of the first and second source/drain regions comprises SiGe.

32. The semiconductor device of claim 28 wherein the substrate has a <110> crystal orientation.

33. The semiconductor device of claim 28 wherein the substrate has a <100> crystal orientation.

34. The semiconductor device of claim 28 wherein the substrate is a silicon-on-insulator substrate.

35. The semiconductor device of claim 28 wherein the substrate is a bulk silicon substrate.

36. The semiconductor device of claim 28 wherein at least one set of the first and second source/drain regions comprises strained source/drain regions.

37. The semiconductor device of claim 28 further comprising an etch stop layer located over the NMOS and PMOS devices and imparting a first stress in the first source/drain regions and a second stress in the second source/drain regions, wherein the first and second stresses are substantially different in magnitude.

38. A semiconductor device, comprising:

an isolation region located in a substrate;

an NMOS device located partially over a surface of the substrate; and

a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface;

wherein a first one of the NMOS and PMOS devices includes one of:

first source/drain regions located at least partially within the substrate and comprising SiC; and

first source/drain regions located at least partially within the substrate and comprising SiGe; and

wherein a second one of the NMOS and PMOS devices includes one of:

second source/drain regions located at least partially within the substrate and comprising SiC wherein the first source/drain regions comprise SiGe;

second source/drain regions located at least partially within the substrate and comprising SiGe wherein the first source/drain regions comprise SiC; and

second source/drain regions located at least partially within the substrate and substantially not comprising either of SiC and SiGe.

39. The semiconductor device of claim 38 wherein the first source/drain regions are recessed within the surface and the second source/drain regions extend from the surface.

40. The semiconductor device of claim 38 wherein:

a high-gate one of the NMOS and PMOS devices includes a first gate interposing associated source/drain regions and having a first height over the surface; and

a low-gate one of the NMOS and PMOS devices includes a second gate interposing associated source/drain regions and having a second height over the surface, wherein the first height is substantially greater than the second height.

41. The semiconductor device of claim 38 wherein:

a wide-spacer one of the NMOS and PMOS devices includes a first gate interposing associated source/drain regions and first spacers on opposing sides of the first gate, the first spacers each extending from the first gate to a first width; and

a narrow-spacer one of the NMOS and PMOS devices includes a second gate interposing associated second source/drain regions and second spacers on opposing sides of the second gate, the second spacers each extending from the second gate to a second width, wherein the first width is substantially greater than the second width.

42. The semiconductor device of claim 38 wherein at least one set of the first and second source/drain regions comprises strained source/drain regions.

43. The semiconductor device of claim 38 further comprising an etch stop layer located over the NMOS and PMOS devices and imparting a first stress in the first source/drain regions and a second stress in the second source/drain regions, wherein the first and second stresses are substantially different in magnitude.

44. A method of manufacturing a semiconductor device, comprising:

forming an isolation region located in a substrate;

forming an NMOS device located partially over a surface of the substrate; and

forming a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface;

wherein a first one of the NMOS and PMOS devices includes one of:

first source/drain regions recessed within the surface; and

first source/drain regions extending from the surface; and

wherein a second one of the NMOS and PMOS devices includes one of:

second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface;

second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and

second source/drain regions substantially coplanar with the surface.

45. The method of claim 44 wherein:

a high-gate one of the NMOS and PMOS devices includes a first gate interposing associated source/drain regions and having a first height over the surface; and

a low-gate one of the NMOS and PMOS devices includes a second gate interposing associated source/drain regions and having a second height over the surface, wherein the first height is substantially greater than the second height.

46. The method of claim 44 wherein:

a wide-spacer one of the NMOS and PMOS devices includes a first gate interposing associated source/drain regions and first spacers on opposing sides of the first gate, the first spacers each extending from the first gate to a first width; and

a narrow-spacer one of the NMOS and PMOS devices includes a second gate interposing associated source/drain regions and second spacers on opposing sides of the second gate, the second spacers each extending from the second gate to a second width, wherein the first width is substantially greater than the second width.

47. An integrated circuit device, comprising:

a plurality of semiconductor devices each including:

an isolation region located in a substrate;

an NMOS device located partially over a surface of the substrate; and

a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface;

wherein, in ones of the plurality of semiconductor devices, a first one of the NMOS and PMOS devices includes one of:

first source/drain regions recessed within the surface; and

first source/drain regions extending from the surface; and

wherein, in ones of the plurality of semiconductor devices, a second one of the NMOS and PMOS devices includes one of:

second source/drain regions recessed within the surface wherein the first source/drain regions extend from the surface;

second source/drain regions extending from the surface wherein the first source/drain regions are recessed within the surface; and

second source/drain regions substantially coplanar with the surface; and

a plurality of interconnects connecting ones of the plurality of semiconductor devices.

48. The integrated circuit device of claim 47 wherein, in each of the plurality of semiconductor devices having one of source/drain regions recessed within the surface and source drain regions extending from the surface:

a high-gate one of the NMOS and PMOS devices includes a first gate interposing associated source/drain regions and having a first height over the surface; and

a low-gate one of the NMOS and PMOS devices includes a second gate interposing associated source/drain regions and having a second height over the surface, wherein the first height is substantially greater than the second height.

49. The integrated circuit device of claim 47 wherein, in each of the plurality of semiconductor devices having one of source/drain regions recessed within the surface and source drain regions extending from the surface:

a wide-spacer one of the NMOS and PMOS devices includes a first gate interposing associated source/drain regions and first spacers on opposing sides of the first gate, the first spacers each extending from the first gate to a first width; and

a narrow-spacer one of the NMOS and PMOS devices includes a second gate interposing associated source/drain regions and second spacers on opposing sides of the second gate, the second spacers each extending from the second gate to a second width, wherein the first width is substantially greater than the second width.